

IN THE CLAIMS:

Please amend Claims 3 to 5, 8, 12 to 14, and 17, and add new Claims 19 and 20, as shown below. The claims, as pending in the subject application, read as follows:

1. (Previously Presented) An annealing method of annealing an SOI substrate, comprising:

holding the SOI substrate in a reducing atmosphere containing hydrogen by a holding portion having a surface formed from silicon and annealing the SOI substrate, wherein the holding portion is a member having a silicon film thereon or a member formed from single-crystal silicon or polysilicon.

2. (Original) The method according to claim 1, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

3. (Currently Amended) The method according to ~~claim 1~~ claim 2, wherein the annealing is executed at a temperature not less than 775°C.

4. (Currently Amended) The method according to ~~claim 1~~ claim 2, wherein the annealing is executed at a temperature not less than 966°C .

5. (Currently Amended) The method according to ~~claim 1~~ claim 2, wherein the annealing is executed at a temperature not less than 993°C.

6. (Previously Presented) An SOI substrate manufactured using an annealing method of claim 1.

7. (Original) The substrate according to claim 6, wherein an HF defect density is not more than 0.05 defects /cm².

8. (Currently Amended) A semiconductor device manufacturing method, comprising the steps of:
annealing an SOI substrate using an annealing method of claim 1; and
forming an active region for a transistor in a ~~nonporous~~ semiconductor layer of the SOI substrate.

9. (Cancelled)

10. (Previously Presented) An annealing method of annealing an SOI, comprising:
holding the SOI substrate in a reducing atmosphere containing hydrogen by a holding portion and annealing the SOI substrate, wherein the holding portion contains no silicon carbide formed by sintering and has a surface formed from silicon carbide deposited by CVD.

11. (Original) The method according to claim 10, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

12. (Currently Amended) The method according to ~~claim 10~~ claim 11, wherein the annealing is executed at a temperature not less than 775°C.

13. (Currently Amended) The method according to ~~claim 10~~ claim 11, wherein the annealing is executed at a temperature not less than 966°C.

14. (Currently Amended) The method according to ~~claim 10~~ claim 11, wherein the annealing is executed at a temperature not less than 993°C .

15. (Previously Presented) An SOI substrate manufactured using an annealing method of claim 10.

16. (Original) The substrate according to claim 15, wherein an HF defect density is not more than 0.05 defects /cm².

17. (Currently Amended) A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of claim 10; and

forming an active region for a transistor in a ~~nonporous~~ semiconductor layer of the SOI substrate.

18. (Cancelled)

19. (New) A semiconductor device manufacturing method, comprising the steps of:

preparing an SOI substrate manufactured using an annealing method of claim 1;

and

forming an active region for a transistor in a semiconductor layer of the SOI substrate.

20. (New) A semiconductor device manufacturing method, comprising the steps of:

preparing an SOI substrate manufactured using an annealing method of claim 10;

and

forming an active region for a transistor in a semiconductor layer of the SOI substrate.